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Reduced Complexity Wallace Multiplier using Parallel Prefix Adders

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Abstract

The design of an area reduced and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. It works on the basis of "Acceleration of addition of summands". The final two rows are summed with a carry propagating adder. A direct implementation requires a (2N-2) bit carry propagating adder, where N – number of bits of operands. The objective of a good multiplier is to provide a physically compact, high speed and low power consuming chip. A system performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. It is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is the major design issue. In this paper we are using reduced complexity Wallace multiplier using parallel prefix adder to speed up the final addition.

Keywords: High speed multipliers, Wallace multiplier, Parallel prefix adder, Sklansky adder, Kogge-Stone adder, Ladner - Fischer adder.

Introduction

In the past, multiplication was generally implemented via a sequence of addition, subtraction and shift operations. Multiplication can be considered as a series of repeated addition. The number to be added is the multiplicand, the number of times it is added is the multiplier and the result is the product. Each step of addition generates a partial product. In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products and the second one collects and adds them.

Proposed Method

In this proposed method, the reduced complexity wallace multiplier is improved by using parallel prefix adder.

A. Reduced Complexity Wallace multiplier:

It is the modified version of Wallace multiplier. It has less half adders than the normal Wallace multiplier .the partial products are formed by

N AND gates. The partial products are arranged in an "inverted triangle" order. The modified Wallace reduction method divides the matrix into three stages.

Stage1:Use full adders for each group of three bits in a column like the conventional Wallace reduction.

Stage2:A group of two bits in a column is not processed, that is, it ispassed on to the next stage(in contrast to conventional method) .Single bits are passed on to the next stage as in the conventional Wallace reduction.

Stage3:The only time half adders are used is to ensure thah the number of stages does not exceed that of a conventional Wallacemultiplier. For some cases, half adders are only used in the final stage of reduction.

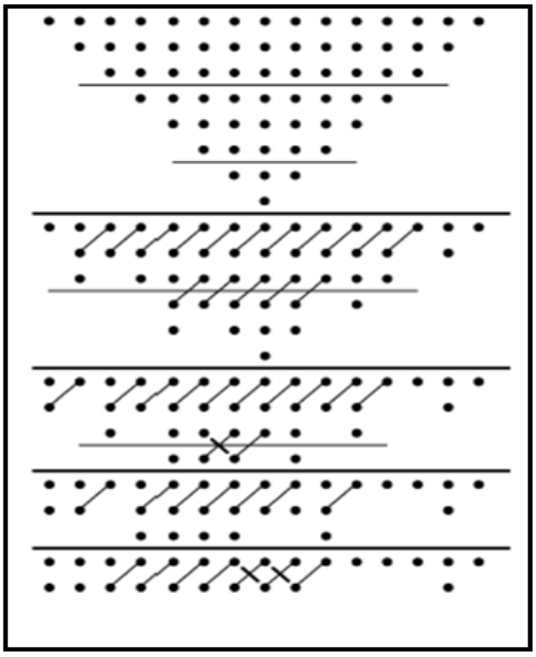


Fig: 1 Dot Notation of Reduced Complexity Wallace Multiplier

B. Parallel Prefix Adder:

The worst case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which can be approximated by:

$$t=(n-1)t_c+t_s$$

t_c is the delay through the carry stage of a full adder and t_s is the delay to compute the sum of the last stage. The delay of ripple carry adder is linearly proportional to n, the number of bits; therefore the performance of the RCA is limited when n grows bigger. The advantage of RCA is lower power consumption as well as a compact layout giving smaller chip area. To design a large adder ripple carry adders are cascaded. As of today standards, it is a common philosophy that area can be traded off in order to achieve higher speed this will be shown in the next section by presenting alternative methods that are based on pre-determining the carry signal of a number of stages based only on the input values.

C. Types of parallel prefix adders:

(i) Sklansky adder:

This is one type of adder. This is used to find the sum and carry of binary inputs. This adder is also called conditional adder. It was proposed in the year 1960. It was invented by J.SKLANSKY. It has minimal depth and high fan out. The main advantage of this logic is that each group computes the partial results in parallel and the multiplexers are ready to give the final result "immediately" with the minimum delay. Thus the maximum delay is reduced in the carry propagation path.

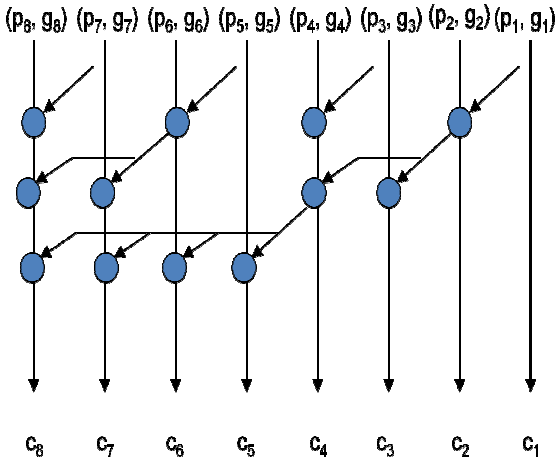


Fig 2 - 8 bit Sklansky Adder's carry generation stage

(ii) Kogge-stone adder:

It is invented in the year 1973. Then compared to sklansky adder kogge stone is better, because kogge stone has reduced area and delay. It has the following advantages like low depth, high node count and minimal fan-out of 1 at each node. It is also known as Conditional Sklansky Adder. The structure of Stage 2 gets changed. It has low depth and high fan out

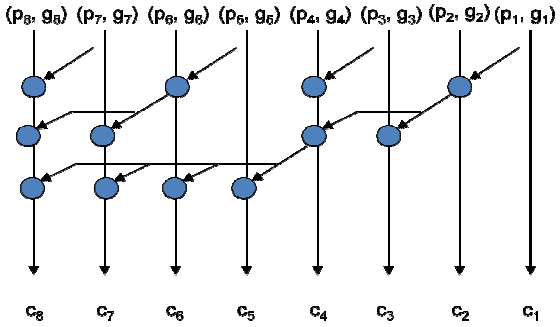


Fig 3 - 8 bit Kogge-Stone Adder's carry generation stage

(iii) Ladner-fischer adder:

It was invented in the year 1980. Compared to kogge-stone delay and area is reduced. The adder topology appears same as the Sklansky conditional adder. In Ladner-fischer adder delay and area is reduced. This adder topology appears the same as the Sklansky conditional sum adder. Ladner-Fischer formulated a parallel prefix network design space which included this minimal depth case. The actual adder they included as an application to their work had a structure that was slightly different. It has Low depth and High fan-out nodes.

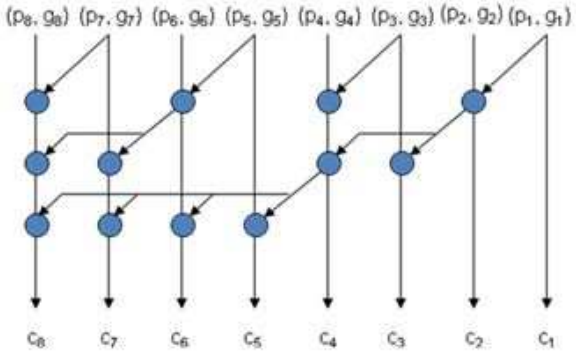


Fig 4 - 8 bit Ladner-fischer Adder's carry generation stage

(iv)Ripple Carry Adder:

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.

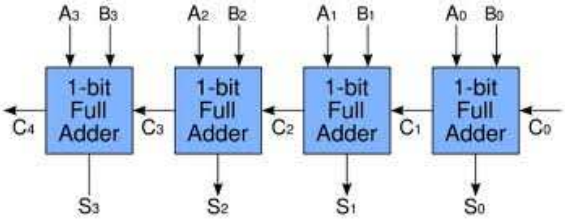


Fig 5 – 4 Bit Ripple Carry Adder

The parallel prefix adder employs three stage structure of CLA adder.

The three stages are as follows

Stage 1: Precalculation of pi (propagation) and gi (generation) terms
Stage2: Calculation of Carry terms. Parallelized ope ration to reduce time
Stage3: Adder to generate the sum

Stage 1: Propagation generation terms & Partial sum;
p(i)=a(i)+b(i)
g(i)=a(i).g(i)
psum (i)=a(i) b(i)
Stage 2: Prefix computation (Carry generation stage)
P [i : j]=P[i : k].P[k-1 : j], if $n \geq i > j \geq 1$
G [i : j]=G[i : k] + (P[i : k] . G [k-1 : j]), if $n \geq i > j \geq 1$
Where n=no. of bits
Stage 3: Final Stage (sum & carry):
C(i)=G [i:1]
Sum(i)=psum (i)c(i-1)

D. Proposed Multiplier structure:

The proposed multiplier will have the stages of the Wallace multiplier in reduction stages. At the final stage where a normal carry propagating adder is present, hence parallel prefix adder is used. In parallel prefix adder the addition process takes place parallely. Delay and power consumption is reduced when compared to the conventional multipliers. Hence the area and power consumption of the wallace multiplier can be reduced by using few number of half adders in the reduction phase and by increasing the usage of full adders.

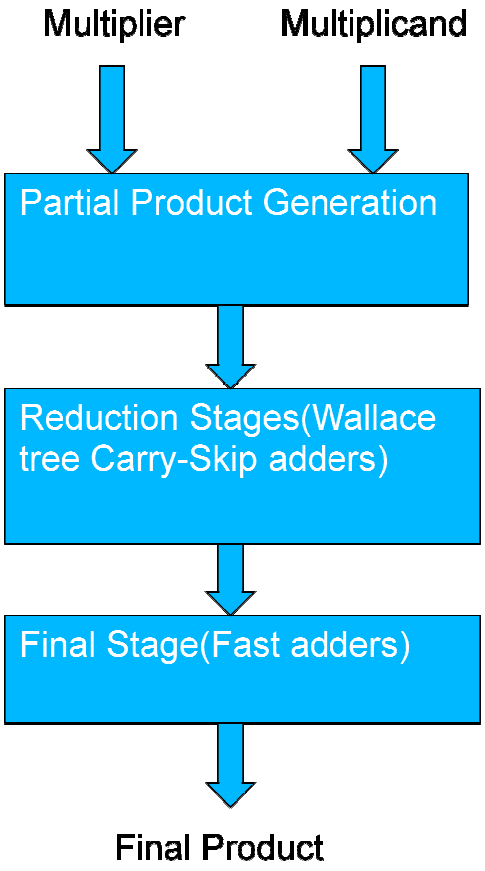


Fig 6.Proposed multiplier structure

The implementation has been done in the VHDL programming languages using Xilinx ISE 10.1 software.Implemented multipliers are:

1) Wallace multiplier – 4bit, 8bit, 16bit
2) Reduced Complexity Wallace multiplier – 4bit, 8bit, 16bit
3) Wallace multiplier with Sklansky adder 8bit, 16bit
4) Reduced Complexity Wallace multiplier with Sklansky adder – 8bit, 16bit

5) Wallace multiplier with Kogge-Stone adder 8bit, 16bit
6) Reduced Complexity Wallace multiplier with Kogge-Stone adder – 8bit, 16bit

Experimental Results

The timing details are collected from the synthesis reportThe sample outputs & timing details are as follows

A. Simulation Output

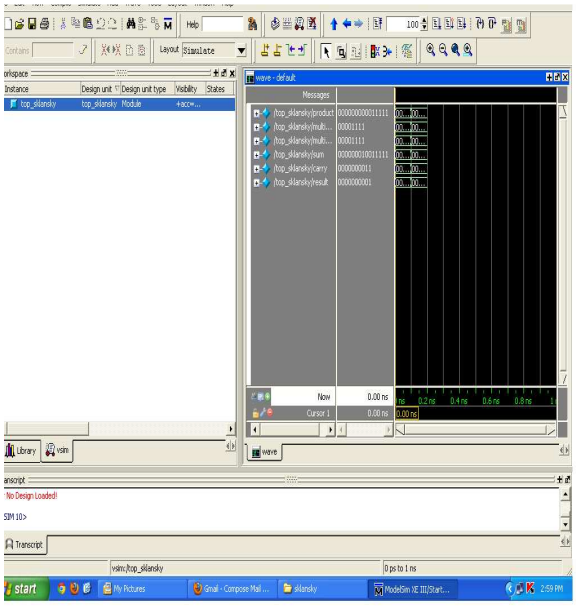
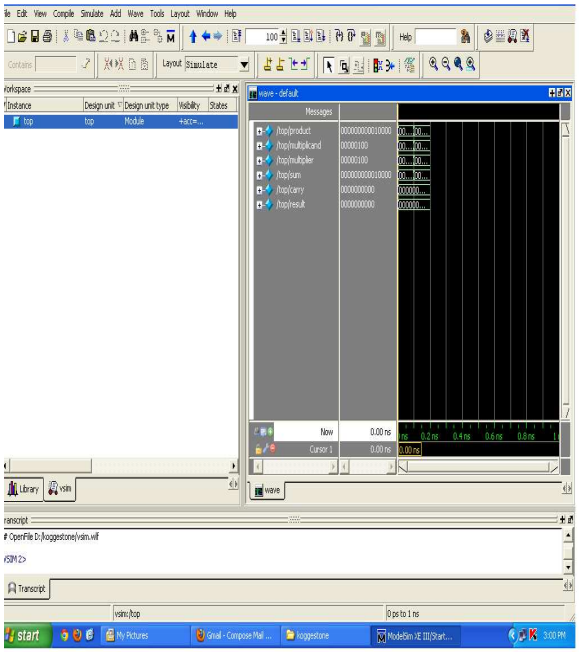


Fig 7 simulation output of sklansky adder



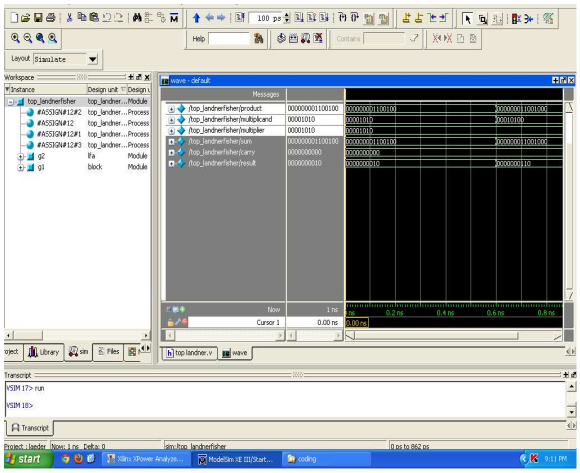


Fig 9 simulation output of Ladner -Fischer adder

B. Performance Analysis

Multipliers	AREA	POWER	DELAY
Reduced Complexity Wallace multiplier with Sklansky adder	LUTs=139 Slices= 75	0.372 W	24.730 ns
Reduced Complexity Wallace multiplier with Kogge-Stone adder	LUTs=155 Slices= 85	0.115 W	21.630 ns
Reduced Complexity Wallace multiplier With Ladner-Fischer adder	LUTs=120 Slices= 63	0.023 W	14.138 ns

Table1.performance Analysis

Conclusion

This paper proposes improvement of Wallace multipliers [Normal & Reduced Complexity] reduced delay using parallel prefix adders at the final stage. From the results, it can be inferred that the proposed multipliers has lesser delay than the conventional multipliers. In processes, where repeated multiplication is done, this multiplier will provides reduced complexity performance.

References

[1] Ron S.Waters, Earl E.Swartzlander"AReducedComplexity Wallacemultiplier reduction" in IEEE transactions on Computers, Aug. 2010.

[2] WhitneyJ.Townsend,Earl E.Swartzlander,JacobA.Abraham "Acomparison of Dadda and Wallace multiplier delays" University of Texas, at Austin,work Under National Sceince foundation graduate research fellowship.

[3] Wallace C. S. " A suggesstion for a fast multiplier " in IEEE transactions on Electronics and Computers, 1964.

[4] Kostas Vitoroulis " parallel prefix adder: notes" Concordia university, 2006.

[5] Taeko Matsunaga and Yuske Matsunaga "Timing constrained Area minimization algorithm for Parallel prefix adders", IEICE transaction fundamentals, Vol.E90-A, No.12,Dec. 2007.

[6] Nuno Roma, Tiago Dias & Leonel Sousa "Fast adder architectures: Modelling and experimental evaluation" IST/INESE – ID, Lisbon, Portugal, project under Portuguese foundation for science and Technology.

[7] David Haris, " A taxamony of parallel prefix networks" , 37th conference on signals and systems and computers, 2003.